Video Module Interface

VMI Specification
Version 1.4

Preliminary Draft (January 30, 1996)

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1 Overview

1.1 Why VMI?

Video Module Interface, VMI, is a standard proposal for connecting a video module, such as an MPEG module, to a "Video Ready" GUI device. The purpose of VMI is to offer a common function set for computer manufacturers and semiconductor suppliers. It is likely that each computer manufacturer will implement the interface differently for value-added product differentiation. However, by agreeing to a common function set, a computer manufacturer can utilize a wider range of semiconductor solutions since they all support VMI.

1.2 What is VMI?

VMI consists of two functional sets - the Core Set and the Optional Set. The core set contains signals that should be supported by any VMI-compliant device. This includes the video, host port, system signals, and the I^2C port. These core set signals and their timing diagrams are clearly defined in this specification.

Realizing that the core set is not sufficient to fully define the interface between the video module and the GUI device, the optional set is proposed. Signals such as the audio port, power, ground, and additional video ports are part of the optional set. Computer manufacturers are encouraged to take the optional set as a reference and define their own set of signals.

Application notes will be available from various semiconductor suppliers to show different implementation examples of VMI. These examples will include the connectors, pin assignments, and other physical specifications.

1.3 Host Port Interface - Mode A and B

A distinct feature of VMI is the definition of a host port. The host port is essential for devices such as MPEG decoders, whereby compressed data and control are transferred through the host port.

Two modes of the host port control signals are defined to accommodate the two prevalent types of interfaces. A VMI-compliant device must support at least one of the two. The support of both Mode A and B is highly recommended for maximum interface flexibility.

1.4 Expandability

Manufacturers are encouraged to make provisions for including multiple modules in the system. The specification of separate host and I^2C ports allows for the addition of separate VMI video conferencing modules, MPEG modules, TV tuner modules, or other devices which make use of these ports. This expandability will allow for greater value-added product differentiation.

2 VMI Signal Description

2.1 Core Set Functional Description

Signal	Type (From Module Side)	Description
Video Port		
VID[7..0]	O	YUV Video Data
PIXCLK	O	Pixel Clock
VACTIVE	O	Video Active
HREF	O	Horizontal Reference
VREF	O	Vertical Reference
I^2C Port		
I2CCLK	I/O	I^2C Clock
I2CDAT	I/O	I^2C Data
Host Port - Mode A		
HD[7..0]	I/O	Host Data Port
HA[3..0]	I	Host Address
CS#	I	Chip Select
DS#	I	Data Strobe
R/W#	I	Read/Write#
DTACK#	O	Data Acknowledge
Host Port - Mode B		
HD[7..0]	I/O	Host Data Port
HA[3..0]	I	Host Address
CS#	I	Chip Select
RD#	I	Read
WR#	I	Write
READY	O	Data Ready
System Signals		
RESET#	I	System Reset
INTREQ#	O	Interrupt Request - Open Drain (CMOS) Open Collector, Level Sensitive (TTL)
INSERT#	O	Card Inserted - When tied to ground this signal indicates that a VMI card has been inserted.

2.2 Core Set Compliance

2.2.1 Existing Silicon

Since many devices will not be fully compliant with existing silicon, it is up to the OEM to verify that devices will work together reliably. Silicon vendors should attempt to achieve compliance when the next versions of silicon are released.

2.2.2 Future Silicon

In the future, VGA Controllers should support all of the Core Set to provide maximum flexibility for attaching VMI modules. For VMI modules, it is not necessary to support all of the Core signals since silicon vendors will choose to implement either the I^2C port or the Host Port depending on the requirements of a given application.

2.2.3 I^2C

When I^2C is implemented, it is not necessary to implement the entire I^2C protocol. This port is intended to support DDC2B and will in many applications be used to for setting up devices. The VGA Controller is intended to be the Master of this port. Multiple Slave devices are allowed.

2.3 Optional Set Functional Description

VMI allocates a variety of optional signals for audio and video support. The digital audio is specified as I^2S; however, the manufacturer is free to use these signals to support EIAJ-340, AES/EBU, S/PDIF, or other formats as needed.

Signal	Type (From Module Side)	Description
Power And Ground		
+5V	-	+5V Power Supply (Multiple)
+3.3V	-	+3.3V Power Supply (Multiple)
+12V	-	+12V Power Supply
GND	-	Ground (Multiple)
Audio (Digital, I^2S)		
SCLK	O	Digital Audio - Serial Clock
LRCK	O	Digital Audio - Left/Right Clock
PCMDATA	O	Digital Audio - PCM Data
Audio (Analog)		
AUDIOL	O	Analog Audio Left
AUDIOR	O	Analog Audio Right
AUDGND	-	Analog Audio Ground
Analog Video		
AVIDY	I	Analog Video Composite OR Luminance
AVIDC	I	Analog Video Chrominance
AVIDGND	-	Analog Video Ground
Reference Clock		
OSC	I	Reference Oscillator
Mode Select Signals		
User-Defined	I/O	User Defined Signals

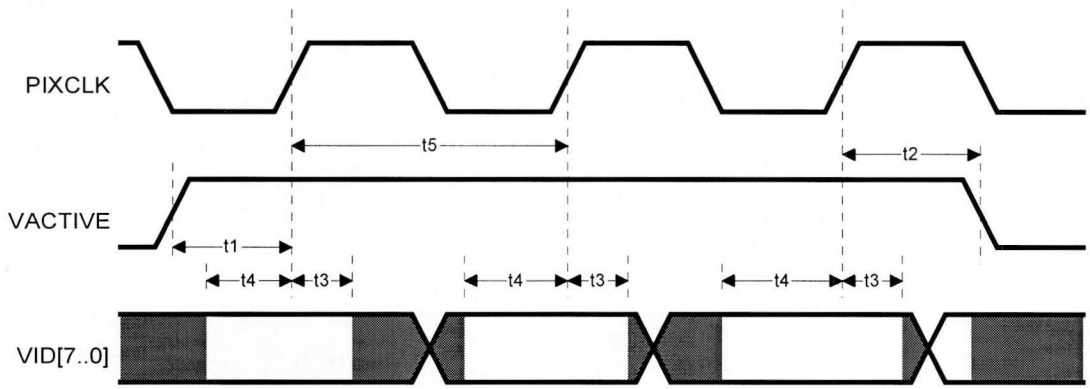
3 Electrical Specification

3.1 Electrical Loading Recommendations

A. Upon power-up, all VMI module outputs should be tristated until a request from the motherboard signals the module to begin driving the bus. The VMI module may continue to drive the bus until a request from the motherboard signals the module to tristate its outputs.

B. Maximum load capacitance per pin should not to exceed 50pF (I^2C Port excluded).

3.2 YUV Port Timing



	Description	MIN (ns)	MAX (ns)
t1	VACTIVE setup to PIXCLK HIGH	5	-
t2	VACTIVE hold after PIXCLK HIGH	0	-
t3	VID hold after PIXCLK HIGH	0	-
t4	VID setup to PIXCLK HIGH	5	-
t5	Cycle Time	35	-

VACTIVE indicates that valid pixel data is being transmitted across the YUV port. Although transitions in VACTIVE are allowed to support common HREF/VREF systems, VACTIVE is intended to allow a hardware mechanism for cropping data.

For systems which do not support a VACTIVE signal, HREF can generally be connected to the VMI VACTIVE signal with a minimal loss of function. If this is done, software will need to perform the cropping which may result in a loss of a few pixels per scan line.

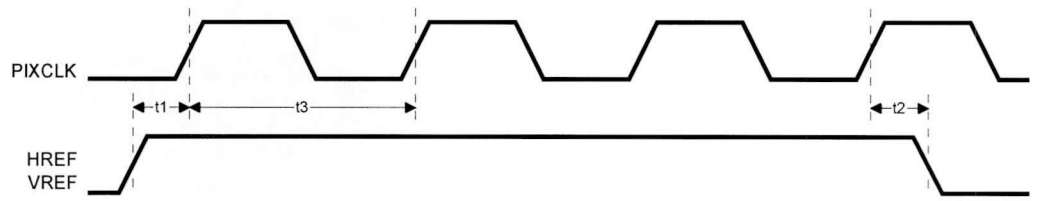
3.2.1 YUV (YCbCr) Byte Ordering

1st byte	2nd byte	3rd byte	4th byte	5th (next DWORD)	6th byte	7th ...
U[7..0]	Y0[7..0]	V[7..0]	Y1[7..0]	U[7..0]	Y0[7..0]	V[7..0]
Cb[7..0]	Y0[7..0]	Cr[7..0]	Y1[7..0]	Cb[7..0]	Y0[7..0]	Cr[7..0]

3.3 HREF/VREF Sync Timing

The timings for HREF and VREF are intended to be consistent with CCIR 601.

3.3.1 Timing



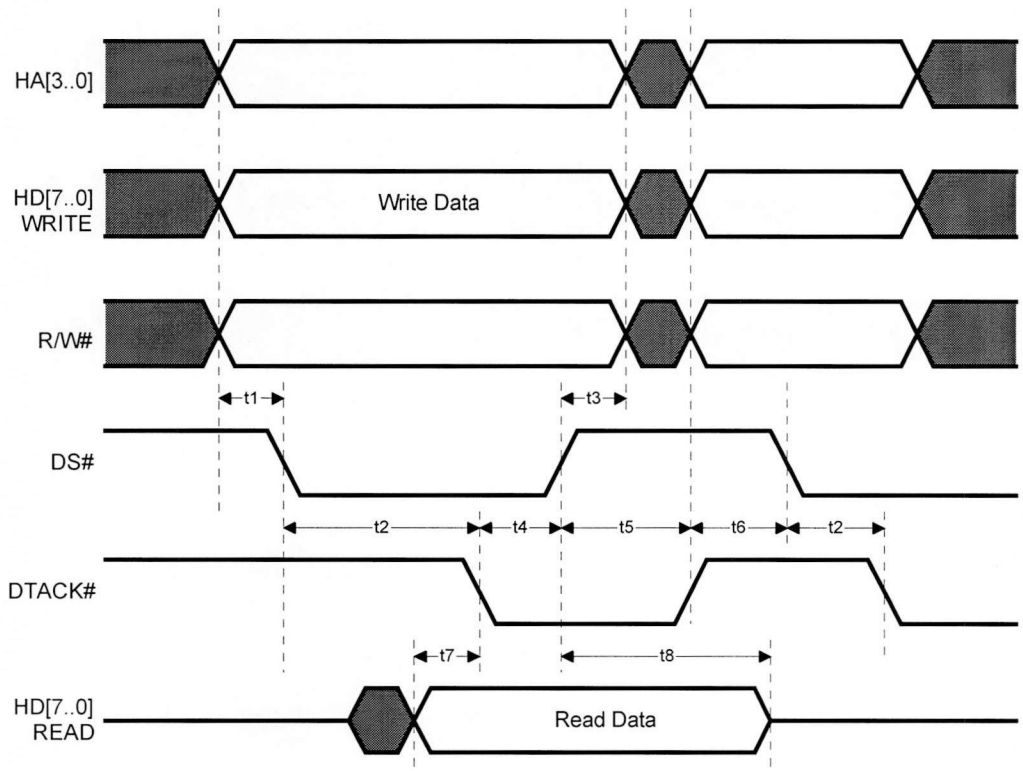
	Description	MIN (ns)	MAX (ns)
t1	HREF/VREF setup to PIXCLK HIGH	5	-
t2	HREF/VREF hold after PIXCLK HIGH	5	-
t3	Cycle time	35	-

3.3.2 Odd/Even Field Detection:

Error! Not a valid filename.

The polarity of the HREF and VREF signals should be programmable by the VGA controller for maximum flexibility. The inactive going edge of the VREF signal indicates whether the field is odd or even. If HREF is active during the falling edge of VREF, the field is EVEN. If HREF is inactive during the falling edge of VREF, the field is ODD.

3.4 Host Port - Mode A Timing

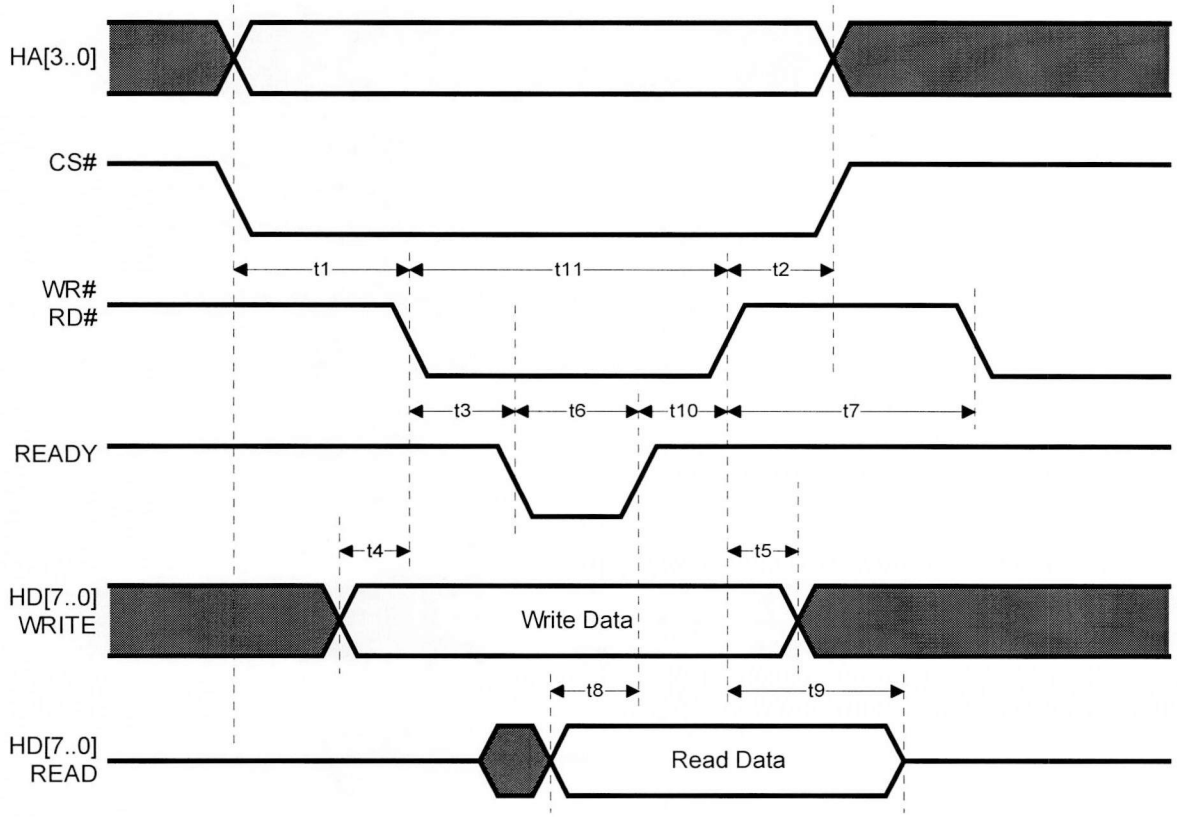


	Description	MIN (ns)	MAX (ns)
t1	HA,HD,R/W# setup until DS# LOW	5	-
t2	Delay DTACK# LOW after DS# LOW	0	13,000[1]
t3	HA,HD,R/W# hold after DS# HIGH	5	-
t4	Delay DS# HIGH after DTACK# LOW	5	100
t5	Delay DTACK# HIGH after DS# HIGH	0	52
t6	Delay DS# LOW (next cycle) after DTACK# HIGH	5	-
t7	(Read Cycle) HD setup until DTACK# LOW	10	-
t8	(Read Cycle) HD hold after DS# HIGH	0	-

The cycle is initiated by the host when DS# transitions LOW. The target responds by pulling DTACK# LOW to indicate that the data has been received or that the requested data is present on the bus. The host then completes its cycle by pulling DS# HIGH. Once the host has completed its cycle, the target pulls DTACK# HIGH to indicate that the operation is complete.

NOTE:
[1] The maximum delay for t2 was chosen to support existing silicon which could delay access to the device for over 500 clocks. This timing is intended to indicate when it is acceptable for the VGA controller to timeout. VMI devices should typically respond within 100ns.

3.5 Host Port - Mode B Timing



	Description	MIN (ns)	MAX (ns)
t1	HA, CS# setup until WR# or RD# LOW	10	-
t2	HA,CS# hold after WR# or RD# HIGH	0	-
t3	Delay READY LOW after WR# or RD# LOW	-	28
t4	HD setup until WR# LOW	5	-
t5	HD hold after WR# HIGH	10	-
t6	READY pulse width	0	-
t7	WR# HIGH until any command	38	-
t8	(Read Cycle) HD setup until READY active	0	-
t9	(Read Cycle) HD hold after RD# inactive	0	15
t10	Delay WR# or RD# HIGH after READY HIGH	0	100
t11	Read/Write command pulse width	40	-

The address and chip select must be presented by the host when the command (WR# or RD#) transitions LOW. If there is no transition on the READY signal within t3(max), then the host will remove the command and complete the operation. If the target is unable to supply or accept data, it must transition READY LOW to delay the cycle.

Note: WR# and RD# cannot both be LOW while CS# is LOW.

Appendix A - VMI Implementation Recommendations

The Video Module Interface defines a set of signals and recommends possible implementations for the motherboard and VMI module. These recommendations are not the only options for manufacturers, but are meant only to serve as a suggestion for developing an appropriate system. The only implementation requirement for a system to be VMI compliant is that it support the Core Set of signals.

A.1 Example 1 - SIMM Socket Implementation

The Video Module Interface may be implemented using a 72 pin, vertical SIMM socket with a 0.050 centerline. These are the same connectors used for memory modules; therefore, the manufacturer will not need to stock a separate component for implementing VMI. In addition to their low cost and wide availability, these connectors allow for additional value-added product differentiation by the OEM since additional user-defined pins are available. The proposed layout groups these extra pins in locations close to the Video and Host data ports to facilitate expansion to 16 bit ports when desired. Pins 8-28 contain the signals from the feature connector to allow the manufacturer to easily route a 26 pin male header next to the SIMM connector for backward compatibility. In addition, the placement of optional analog signals was carefully selected to help eliminate possible noise problems.

A.1.1 Proposed SIMM Socket Pin Definition

72 pin SIMM socket, 0.050 in. centers			
Pin #	**VMI Signal**	**Pin #**	**VMI Signal**
1	12V	**37**	User-Defined
2	Ground	**38**	User-Defined
3	3.3V	**39**	Ground
4	User-Defined	**40**	HA[0]
5	User-Defined	**41**	HA[1]
6	User-Defined	**42**	HA[2]
7	User-Defined	**43**	HA[3]
8	VID[0]	**44**	Ground
9	VID[1]	**45**	5V
10	VID[2]	**46**	HD[0]
11	VID[3]	**47**	HD[1]
12	Ground	**48**	HD[2]
13	3.3V	**49**	HD[3]
14	VID[4]	**50**	Ground
15	VID[5]	**51**	3.3V
16	VID[6]	**52**	HD[4]
17	VID[7]	**53**	HD[5]
18	Ground	**54**	HD[6]
19	5V	**55**	HD[7]
20	VACTIVE	**56**	Ground
21	VREF	**57**	OSC
22	HREF	**58**	3.3V
23	3.3V	**59**	WR# (R/W#)
24	Ground	**60**	RD# (DS#)
25	PIXCLK	**61**	READY (DTACK#)
26	I2CCLK	**62**	CS#
27	INTREQ#	**63**	Ground
28	I2CDAT	**64**	User-Defined
29	PCMDATA	**65**	User-Defined/AVIDY
30	LRCK	**66**	User-Defined/AVIDC
31	SCLK	**67**	User-Defined/AVIDGND
32	Ground	**68**	INSERT#
33	5V	**69**	RESET#
34	User-Defined	**70**	AUDGND
35	User-Defined	**71**	AUDIOL
36	User-Defined	**72**	AUDIOR

A.2 Example 2 - Feature Connector Implementation

VMI could be implemented as a superset of the feature connector. The 26 pin male header (connector A) could be modified to support the Video Port and I^2C Port. The addition of a 40 pin female receptacle (connector B) would add support for the Host Port and other optional signals. This recommendation of separate male and female connectors and the use of a plug in the receptacle will help to prevent incorrect assembly of the VMI module. With this configuration, it is still possible to misalign the card by one row. If this is unacceptable, the manufacturer could choose to use a shrouded connector.

A.2.1 Proposed Video Port Implementation on the Feature Connector

CONNECTOR A (26 Pin Male Dual Row Header, 0.100 in. centers)						
Standard Feature Connector		Video Port Implementation		Standard Feature Connector		Video Port Implementation
Pin #	Signal Name	Signal Name		Pin #	Signal Name	Signal Name
Z1	Ground	Ground		Y1	P0	VID[0]
Z2	Ground	Ground		Y2	P1	VID[1]
Z3	Ground	Ground		Y3	P2	VID[2]
Z4	EVIDEO#	VACTIVE		Y4	P3	VID[3]
Z5	ESYNC#	User-Defined		Y5	P4	VID[4]
Z6	EDCLK#	VREF		Y6	P5	VID[5]
Z7	N/C	I2CCLK		Y7	P6	VID[6]
Z8	Ground	Ground		Y8	P7	VID[7]
Z9	Ground	Ground		Y9	DCLK	PIXCLK
Z10	Ground	Ground		Y10	BLANK#	HREF
Z11	Ground	Ground		Y11	HSYNC	N/C
Z12	N/C	User-Defined		Y12	VSYNC	N/C
Z13	N/C	I2CDAT		Y13	Ground	Ground

A.2.2 Proposed VMI Host Port Implementation

Connector B was chosen to have 40 pins to allow for future expansion and to provide manufacturers and suppliers with additional flexibility. A number of signals are currently listed as User-Defined and may be used to support additional signals.

CONNECTOR B (40 Pin Female Dual Row Receptacle, 0.100 in. centers)			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
Z1	+12v	Y1	HD[0]
Z2	HD[1]	Y2	Ground
Z3	Ground	Y3	HD[2]
Z4	HD[3]	Y4	HD[4]
Z5	+5V	Y5	HD[5]
Z6	HD[6]	Y6	HD[7]
Z7	OSC	Y7	HA[0]
Z8	HA[1]	Y8	HA[2]
Z9	HA[3]	Y9	+5V
Z10	Ground	Y10	RESET#
Z11	CS#	Y11	Ground
Z12	RD#	Y12	WR#
Z13	+3.3V	Y13	READY
Z14	SCLK	Y14	INTREQ#
Z15	LRCK	Y15	PCMDATA
Z16	+5V	Y16	+3.3V
Z17	User-Defined	Y17	User-Defined
Z18	User-Defined	Y18	KEY
Z19	INSERT#	Y19	AUDIOL
Z20	AUDGND	Y20	AUDIOR

A.2.3 Optional Host Port - Mode A Signals

Pin #	Signal	Description
Z12	DS#	Data Strobe
Y12	R/W#	Read/Write#
Y13	DTACK#	Data Acknowledge

A.2.4 Recommended Signal Description for Future Analog Video Expansion

Pin #	Signal	Description
Y17	AVIDY	Analog Video Composite or Luminance
Z17	AVIDGND	Analog Video Ground
Z18	AVIDC	Analog Video Chrominance

Appendix B - Layout Recommendation

B.1 Overview

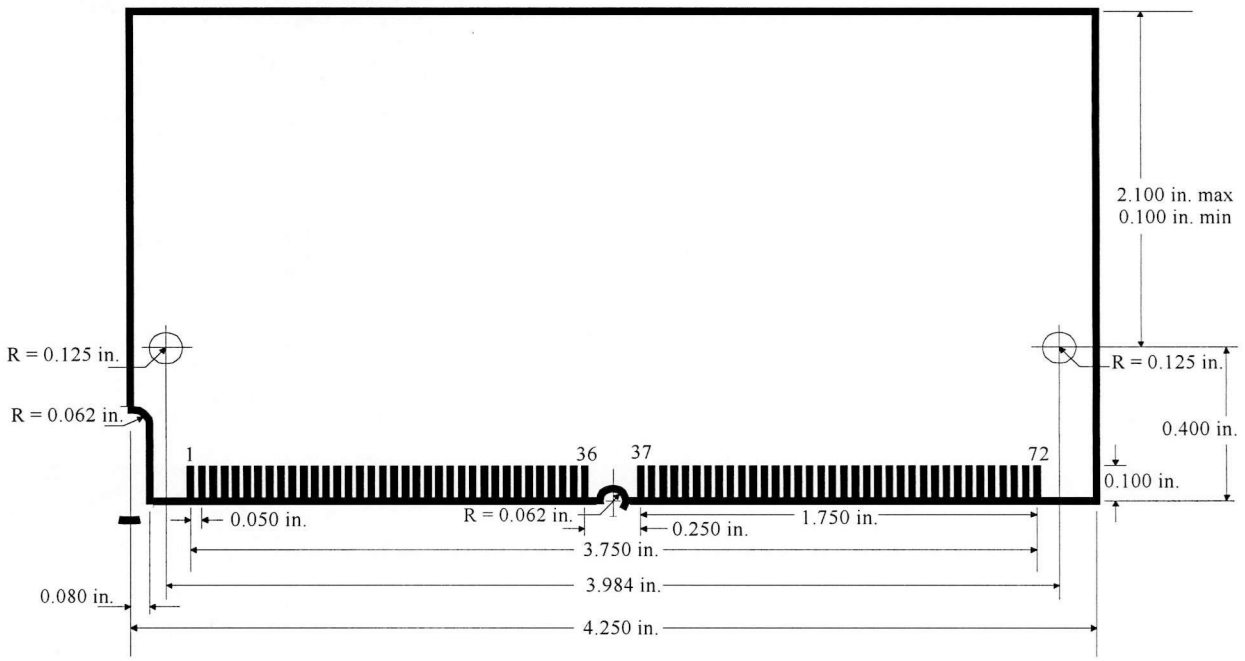
The size of the video module will vary depending on the supplier's actual board layout and component counts. Current video cards are often built on boards as large as 8.5 inches by 4.0 inches. Although it is likely that most module would be considerably smaller, it is conceivable for modules to grow to this size as their complexity increases. For this reason, the video module has been defined to have a maximum board size of 8.500 inches by 4.000 inches. This size is not a problem when standard dual-row headers are used. However, it is important to realize that the implementation chosen will effect maximum card sizes.

B.2 Layout Options

B.2.1 Example 1 - Using a 72 pin SIMM Socket

If VMI is implemented using a SIMM socket, the manufacturer will need to work with suppliers to determine maximum card sizes for the specific connectors used to insure that the connectors will be reliable. It is recommend that the VMI card not exceed 2.5 inches in height for this implementation. Care should also be taken to place larger components close to the bottom edge of the VMI card to relieve strain on these connectors.

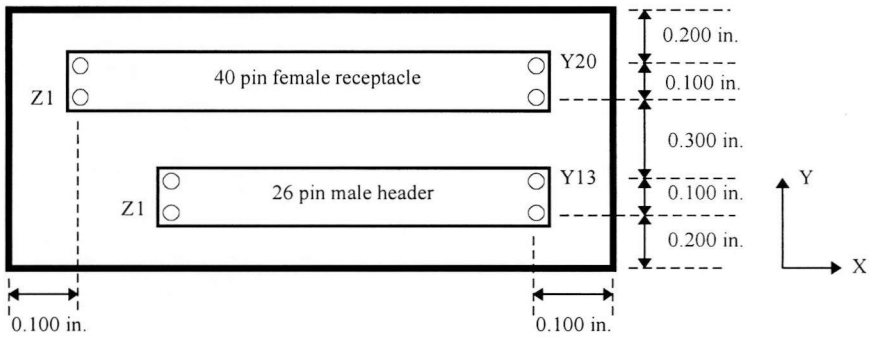
View: Looking at component side of VMI card



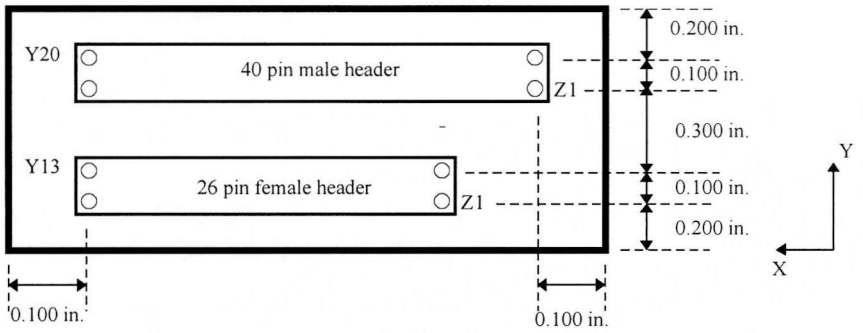
B.2.2 Example 2 - Feature Connector Implementation on an Adapter Card

If VMI is implemented on an adapter card, compact modules can be obtained by aligning the connectors vertically and placing the components facing each other. Placement of components should be done carefully to avoid height limitations and overheating problems

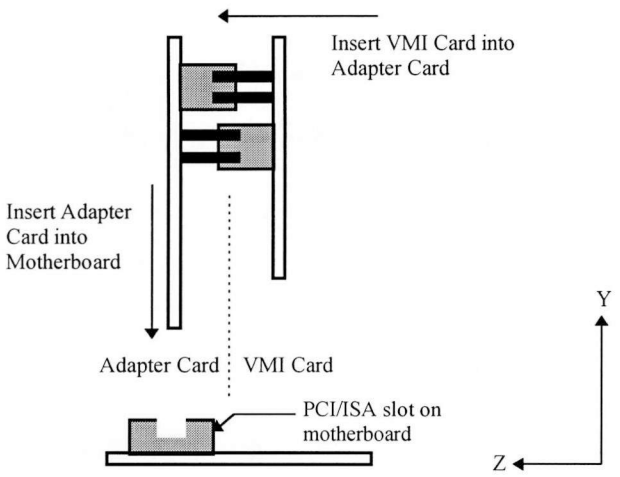
View: Looking at component side of the adapter card



View: Looking at component side of the VMI Daughter Card



View: Looking along length of connectors

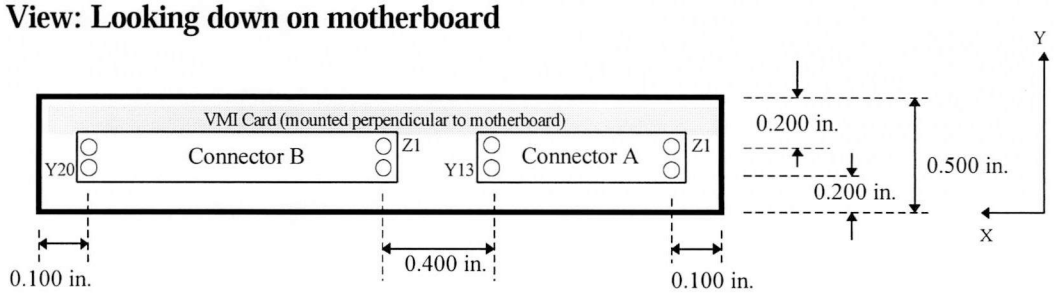


B.2.3 Example 3 - Feature Connector Implementation on a Motherboard

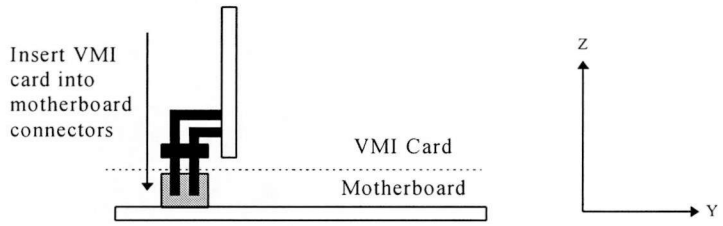
Although the manufacturer is free to choose his own placement for the connectors, it is recommended that the connectors be aligned along their width so that the VMI cards may be mounted perpendicular to the motherboard. It is further suggested that space be allocated for the VMI card to expand beyond connector B. The following figures detail the placement of the connectors on the motherboard and VMI card, but are only meant to serve as a suggestion. The manufacturer is free to work with suppliers to select an appropriate orientation, and is encouraged to do so.

No component side has been specified for the VMI card, but it is advantageous to place components which extend off the VMI card over one of the connectors to avoid height limitations from components on the motherboard.

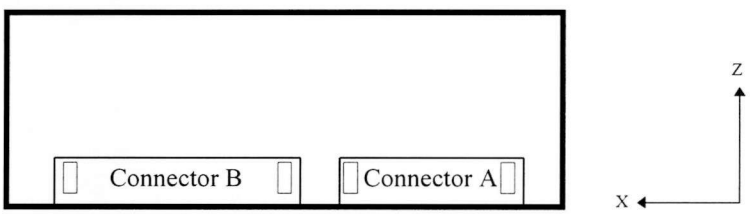
View: Looking down on motherboard



View: Looking along length of connectors



View: Looking at VMI Card



NOTE: VMI cards may extend in the Z direction up to 4.000 inches and in the X direction up to 8.500 inches.

Appendix C - Connector Recommendation

C.1 Example 1 - SIMM Socket Implementation

Supplier	Part Number
BERG Electronic	92247-113
AMP	822031-4

C.2 Example 2 - Feature Connector Implementation on an Adapter Card

	Part Number			
	Connector A		Connector B	
Supplier	Adapter card (male)	Video Module (female)	Adapter card (female)	Video Module (male)
BERG Electronic	67997-426	68683-613	68683-320	67997-540
AMP	1-103186-3	1-535598-3	2-535598-3	2-103186-0

C.3 Example 3 - Feature Connector Implementation on a Motherboard

	Part Number			
	Connector A		Connector B	
Supplier	Motherboard (male)	Video Module (female)	Motherboard (female)	Video Module (male)
BERG Electronic	67997-426	66925-013	68683-320	79257-440
AMP	1-103186-3	1-146140-2	2-535598-3	2-103326-0